Electronics in particle physics

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Electronics in experiments

- A lot of electronics in the experiments...
  - Readout electronics: amplification, filtering...: **Analog electronics (A,V,C)**
  - Processing & Trigger electronics: **Digital electronics (bits)**
  - The performance of electronics often impacts on the detectors
Electronics allowing better detectors: trackers

- Measurement of (charged) particle tracks
  - millions of pixels (~100 μm)
  - (quasi) binary readout at 40 MHz
  - High radiation levels
  - Made possible by ASICs

Tracks in an e+e- collision at ILC

Pixel detector and readout electronics
Importance of electronics: calorimeters

- **Calorimetry** = energy measurement (≈ mass)
- **Dynamic range**: maximum signal/minimum signal (or noise)
  - Typically: $10^3 - 10^5$
  - Often specified in dB ($=20\log \frac{V_{\text{max}}}{V_{\text{min}}}$) = 60 – 100 dB
  - Also in bits: $2^n = \frac{V_{\text{max}}}{V_{\text{min}}} = 10 – 18$ bits
- **Precision ~1%**
  - Energy resolution: $\sigma(E)$
  - Importance of low noise, uniformity, linearity...

H→γγ in CMS calorimeter

- [F. Gianotti, CERN summer students 2003]
**Overview of readout electronics**

- **Most front-ends follow a similar architecture**

![Diagram of readout electronics architecture](image)

- Very small signals (fC) -> need amplification
- Measurement of amplitude and/or time (ADCs, discris, TDCs)
- Several thousands to millions of channels
Readout electronics: requirements

- Low noise
- Low power
- High speed
- High reliability
- Radiation hardness
- Large dynamic range
- Low material
- Low cost!
  (and even less)
Detector(s)

- A large variety
- A similar modelization

6x6 pixels, 4x4 mm²
HgTe absorbers, 65 mK
12 eV @ 6 keV

CMS Pixel module

PMT for Antares

ATLAS LAr em calorimeter
Detector modelization

- **Detector = capacitance \( C_d \)**
  - Pixels: 0.1-10 pF
  - PMs: 3-30 pF
  - Ionization chambers: 10-1000 pF
  - **Capa or transmission line?**

- **Signal: current source**
  - Pixels: \( \sim 100 e^-/\mu m \)
  - PMs: 1 photoelectron \( \rightarrow 10^5-10^7 e^- \)
  - Modelized as an impulse (Dirac):
    \[
    i(t) = Q_0 \delta(t)
    \]

- **Missing:**
  - High Voltage bias
  - Connections, grounding
  - Neighbours
  - Calibration...

Diagram: A circuit diagram with labels for \( I \) in and \( C_d \).

Graph: A graph showing a typical PM signal with markers for 200 mV and 100 mV.
Reading the signal

Signal
- Signal = current source
- Detector = capacitance $C_d$
- Quantity to measure
  - Charge $\Rightarrow$ integrator needed
  - Time $\Rightarrow$ discriminator + TDC

Integrating on $C_d$
- Simple : $V = \frac{Q}{C_d}$
- « Gain » : $\frac{1}{C_d}$ : 1 pF $\rightarrow$ 1 mV/fC
- Need a follower to buffer the voltage...
- Input follower capacitance : $C_a // C_d$
- Gain loss, possible non-linearities
- crosstalk
- Need to empty $C_d$...
Monolithic active pixels

Epitaxial layer forms sensitive volume (2-20 μm)

Charge collection by diffusion

Charge collected by N-well

Column-parallel ADCs

Data processing / Output stage

I2C control

Readout control

Maps readout

© R Turchetta RAL
Ideal charge preamplifier

- **Ideal opamp in transimpedance**
  - Shunt-shunt feedback
  - transimpedance: \( v_{\text{out}}/i_{\text{in}} \)
  - \( \text{Vin}=0 \Rightarrow v_{\text{out}}(\omega)/i_{\text{in}}(\omega) = -Z_f = -1/j\omega C_f \)
  - **Integrator**: \( v_{\text{out}}(t) = -1/C_f \int i_{\text{in}}(t) dt \)
    
    \[ v_{\text{out}}(t) = -Q/C_f \]

- \( \text{« Gain »}: 1/C_f : 0.1 \text{ pF} \rightarrow 10 \text{ mV/fC} \)
- \( C_f \) determined by maximum signal

- **Integration on \( C_f \)**
  - Simple: \( V = -Q/C_f \)
  - Unsensitive to preamp capacitance \( C_{\text{PA}} \)
  - Turns a short signal into a long one
  - The front-end of 90% of particle physics detectors...
  - But always built with custom circuits...
Non-ideal charge preamplifier

- **Finite opamp gain**
  - \( V_{\text{out}}(\omega)/i_{\text{in}}(\omega) = -Z_f / (1 + C_d / G_0 C_f) \)
  - Small signal loss in \( C_d / G_0 C_f \ll 1 \) (ballistic deficit)

- **Finite opamp bandwidth**
  - First order open-loop gain
  - \( G(\omega) = G_0/(1 + j \omega/\omega_0) \)
    - \( G_0 \): low frequency gain
    - \( G_0\omega_0 \): gain bandwidth product

- **Preamp risetime**
  - Due to gain variation with \( \omega \)
  - Time constant: \( \tau (\text{tau}) = C_d / G_0\omega_0 C_f \)
  - Rise-time: \( t_{10-90\%} = 2.2 \tau \)
  - Rise-time optimised with \( w_C \) or \( C_f \)

---

**OPEN-LOOP FREQUENCY RESPONSE**

- Gain
- Phase
- Margin = 60°

**Impulse response with non-ideal preamp**

Cf=0.10pF C=10fC f_c=160MHz
Charge preamp seen from the input

- **Input impedance with ideal opamp**
  - $Z_{in} = Z_f / G+1$
  - $Z_{in} \to 0$ for ideal opamp
  - « Virtual ground » : $V_{in} = 0$
  - Minimizes sensitivity to detector impedance
  - Minimizes crosstalk

- **Input impedance with real opamp**
  - $Z_{in} = 1/j\omega G_0 C_f + 1 / G_0 \omega_0 C_f$
  - Resistive term : $R_{in} = 1 / G_0 \omega_0 C_f$
    - Exemple : $w_c = 10^9$ rad/s $C_f = 0.1$ pF $\Rightarrow R_{in} = 10$ k
  - Determines the input time constant : $t = R_{eq} C_d$
  - Good stability = (...!)

- **Equivalent circuit**

---

Zin = Input impedance or charge preamp

Input impedance or charge preamp

Exemple : $C_f = 2$ pF

$G(\omega)$

$Z_{in}$

$t = \frac{R_{eq} C_d}{G_0}$

$R = \frac{R_x}{G_0}$

$C_d = 10$ pF

$R_f = 100$ k\(\Omega\)

$100$ \(\mu\)H

$R_x = \frac{R_x}{G_0}$
Crosstalk

- Capacitive coupling between neighbours
  - Crosstalk signal is differentiated and with same polarity
  - Small contribution at signal peak
  - Proportionnal to $\frac{C_x}{C_d}$ and preamp input impedance
  - Slowed derivative if $R_i N_d \sim t_p \Rightarrow$ non-zero at peak

- Inductive coupling
  - Inductive common ground return
  - “Ground apertures” = inductance
  - Connectors : mutual inductance
Electronics noise

- Definition of Noise
  - Random fluctuation superposed to interesting signal
  - Statistical treatment

- Three types of noise
  - Fundamental noise (Thermal noise, shot noise)
  - Excess noise (1/f ...)
  - Parasitics -> EMC/EMI (pickup noise, ground loops...)

![Graph showing amplitude over time](image-url)
Electronics noise

- **Modelization**
  - Noise generators: $e_n, i_n$
  - Noise spectral density of $e_n$ & $i_n$: $S_v(f)$ & $S_i(f)$
  - $S_v(f) = |\mathcal{F}(e_n)|^2 (V^2/Hz)$

- **Rms noise $V_n$**
  - $V_n^2 = \int e_n^2(t) \, dt = \int S_v(f) \, df$
  - White noise ($e_n$): $V_n = e_n \sqrt{\frac{1}{2}\pi f_{-3dB}}$
Calculating electronics noise

- **Fundamental noise**
  - Thermal noise (resistors): $S_V(f) = 4kTR$
  - Shot noise (junctions): $S_I(f) = 2qI$

- **Noise referred to the input**
  - All noise generators can be referred to the input as 2 noise generators:
    - A voltage one $e_n$ in series: **series noise**
    - A current one $i_n$ in parallel: **parallel noise**
  - Two generators: no more, no less... why?
    - To take into account the Source impedance

- **Golden rule**
  - Always calculate the signal before the noise
    - what counts is the signal to noise ratio
  - Don’t forget noise generators are $V^2/Hz$ ⇒ calculations in module square
  - Practical exercise next slide
Noise in charge pre-amplifiers

- **2 noise generators at the input**
  - Parallel noise: \( (i_n^2) \) (leakage currents)
  - Series noise: \( (e_n^2) \) (preamp)

- **Output noise spectral density**:
  - \( S_v(\omega) = \left( \frac{i_n^2 + e_n^2}{|Z_d|^2} \right) / \omega^2 C_f^2 \)
    \[ = \frac{i_n^2}{\omega^2 C_f^2} + \frac{e_n^2 C_d^2}{C_f^2} \]
  - Parallel noise in \(1/\omega^2\)
  - Series noise is flat, with a « noise gain » of \(C_d/C_f\)

- **rms noise** \( V_n \)
  - \( V_n^2 = \int S_v(\omega) \, d\omega / 2\pi \to \infty \) (!)
  - Benefit of shaping…

![Diagram of noise in charge pre-amplifiers](image_url)
Equivalent Noise Charge (ENC) after CRRC\textsuperscript{n}

- Noise reduction by optimising useful bandwidth
  - Low-pass filters (RC\textsuperscript{n}) to cut-off high frequency noise
  - High-pass filter (CR) to cut-off parallel noise
  - $\rightarrow$ pass-band filter CRRC\textsuperscript{n}

- Equivalent Noise Charge : ENC
  - Noise referred to the input in electrons
  - $\text{ENC} = I_a(n) e_n C_t / \sqrt{T} \oplus I_b(n) i_n / \sqrt{T}$
  - Series noise in $1/\sqrt{T}$
  - Parallel noise in $\sqrt{T}$
  - 1/f noise independant of $T$
  - Optimum shaping time $\tau_{opt} = \tau_c / \sqrt{2n-1}$

- Peaking time $tp$ (5-100%)
  - ENC($tp$) independent of $n$

- Complex shapers are obsolete :
  - Power of digital filtering
  - Analog filter = CRRC ou CRRC\textsuperscript{2}
Equivalent Noise Charge (ENC) after CRRC$^n$

A useful formula: ENC (e- rms) after a CRRC$^2$ shaper:

$$\text{ENC} = 174 \frac{e_n}{\sqrt{\text{tp}}} C_{\text{tot}} \left( \delta \right) + 166 \frac{i_n}{\sqrt{\text{tp}}} \left( \delta \right)$$

- $e_n$ in nV/√Hz, $i_n$ in pA/√Hz are the preamp noise spectral densities
- $C_{\text{tot}}$ (in pF) is dominated by the detector ($C_d$) + input preamp capacitance ($C_{PA}$)
- $\text{tp}$ (in ns) is the shaper peaking time (5-100%)

Noise minimization

- Minimize source capacitance
- Operate at optimum shaping time
- Preamp series noise ($e_n$) best with high transconductance ($g_m$) in input transistor
  => large current, optimal size

![Graph showing ENC (rms e-) vs. tp (ns) with Series and Parallel configurations]

$C_d = 10\text{pF} \quad e_n = 1\text{nV}/\sqrt{\text{Hz}} \quad i_n = 10\text{fA}/\sqrt{\text{Hz}}$
ENC for various technologies

- ENC for $C_d=1$, 10 and 100 pF at $I_d = 500$ µA
- MOS transistors best between 20 ns - 2 µs

### Parameters

- **Bipolar**:
  - $g_m = 20$ mA/V
  - $R_{BB}=25$ Ω
  - $e_n = 1$ nV/√Hz
  - $I_B=5$ uA
  - $i_n = 1$ pA/√Hz
  - $C_{PA}=100$ fF

- **PMOS 2000/0.35**:
  - $g_m = 10$ mA/V
  - $e_n = 1.4$ nV/√Hz
  - $C_{PA}=5$ pF
  - $1/f$:
MOS input transistor sizing

- Capacitive matching: strong inversion
  - $g_m$ proportional to $W/L \sqrt{I_D}$
  - $C_{GS}$ proportional to $W*L$
  - ENC proportional to $(C_{det}+C_{GS})/\sqrt{g_m}$
  - Optimum $W/L: C_{GS} = 1/3 C_{det}$
  - Large transistors are easily in moderate or weak inversion at small current

- Optimum size in weak inversion
  - $g_m$ proportional to $I_D$ (indep of $W, L$)
  - ENC minimal for $C_{GS}$ minimal, provided the transistor remains in weak inversion
Current preamplifiers:

- **Transimpedance configuration**
  - \( V_{out}(\omega)/i_{in}(\omega) = - \frac{R_f}{1+Z_f/GZ_d} \)
  - **Gain** = \( R_f \)
  - **High counting rate**
  - Typically optical link receivers

- **Easily oscillatory**
  - Unstable with capacitive detector
  - **Inductive** input impedance
    - \( L_{eq} = \frac{R_f}{\omega C} \)
  - Resonance at : \( f_{res} = \frac{1}{2\pi} \sqrt{L_{eq}C_d} \)
  - **Quality factor** : \( Q = \frac{R}{\sqrt{L_{eq}/C_d}} \)
    - \( Q > 1/2 \) -> ringing
  - Damping with capacitance \( C_f \)
    - \( C_f = 2 \sqrt{C_d/R_f G_0\omega_0} \)
    - Easier with fast amplifiers
High speed transimpedance amplifier

- Fast transimpedance amplifiers
  - \( R_f = 25k \), \( C_f = 10fF \)
  - SiGe process
  - 15 GHz gain-bandwidth product

- 40 Gb/s transimpedance for optical
  - Simple architecture (CE + CC)
  - SiGe bipolar transistors
  - CC outside feedback loop
  - « pole splitting »

Open loop frequency response of SiGe amplifier
Charge vs Current preamps

- **Charge preamps**
  - Best noise performance
  - Best with short signals
  - Best with small capacitance

- **Current preamps**
  - Best for long signals
  - Best for high counting rate
  - Significant parallel noise

- **Charge preamps are not slow, they are long**
- **Current preamps are not faster, they are shorter (but easily unstable)**
ADCs : G.D.A.S.A.P.

The era of G.D.A.S.A.P. : « go digital as soon as possible »
- Spectacular evolution of ADCs: more bits, faster, less watts
- Propelled by evolution of technologies and telecom
- Has revolutionized signal processing
- Now coming inside the ASICs

Resolution vs speed of ADCs in 2002
© L. Dugoujon STm
Analog memories

- **Switched Capacitor Arrays (SCAs)**
  - Store signal on capacitors (~pF)
  - Fast write (~GHz)
  - Slower read (~10MHz)
  - Dynamic range: 10-13 bits
  - Depth: 100-2000 caps
  - Unsensitive to cap absolute value (voltage write, voltage read)
  - Low power
  - Possible loss in signal integrity (droop, leakage current)

- **The base of 90% of digital oscilloscopes!**
The MATACQ chip: an oscilloscope on a chip

- Based on the Sampling Matrix principle: evolution of the sampling DLL technique.
- Also includes 10ps precision TAC for trace synchronisation..
- AMS 0.8µm technology
- 2560 samples.
- < 1µs readout time.
- 50 MS/s-2GS/s range.
- 300 MHz Bandwidth.
- 13.5 bit rms dynamic range
- Jitter < 30 ps rms.

- used in the MATACQ (CAEN V1729) board.
- used to read fast photodetectors in small scale experiments or test benches

IEEE TNS 52-6:2853-2860, 2005
Digital filtering

- Linear sums of sampled signal
  - Finite Impulse Response (FIR)
  - made possible by fast ADCs (or analog memories)...

- Signal: \( s(t) = A g(t) + b \)
  - \( A \): amplitude
  - \( G(t) \): normalised signal shape
  - \( B \): noise
  - Sampled signal: \( s_i = A g_i + b_i \)

- Filter: weighted sum \( \sum a_i s_i \)
  - \( a_i = \sum R^{-1}_{ij} g_i \)
  - \( R \): autocorrelation function
  - \( g_i \): signal shape
    - \((0, 0.63, 1, 0.8, 0.47)\)
  - \( S = \sum_{i=1}^{n} a_i s_i \)
Exemple : ATLAS “multiple sampling”

- **Slowing down the signal**
  - Reduction of series noise
  - Similar to a simple integration

- **Accelerating the signal**
  - Reduction of pileup noise
  - Similar to a differentiation

- Measuring the timing

- Some questions
  - How does it compare to an analog filter
  - How many samples are needed?
  - What accuracy is needed on the waveform and on the autocorrelation?
  - What analog shaping time is needed?
  - Is the analog filter really useful?

Signal before and after digital filtering

\[ \text{A} = (0.17, 0.34, 0.4, 0.31, 0.28) \]

\[ \text{A} = (-0.75, 0.47, 0.75, 0.07, -0.19) \]
(R)evolution of analog electronics (1)

- Acces to microelectronics

Charge preamp in SMC hybrid techno

Charge preamp in 0.8µm BiCMOS
(R)evolution of analog electronics (2)

- **ASICs**: Application Specific Integrated Circuits
  - Access to foundries through *multiproject runs* (MPW)
  - Reduced development costs: 600-1000 €/mm² compared to dedicated runs (50-200 k€)
  - Full custom layout, at transistor level
  - Mostly *CMOS & BiCMOS*

- Very widespread in high Energy Physics
  - High level of integration, limited essentially by power dissipation and parasitic couplings (EMC)
  - Better *performance*: reduction of parasitics
  - Better *reliability* (less connections)
  - But *longer development time*
Processing of ASICs

- From Sand to ICs...

Reticle (Pattern with 0.7 micron apertures ie 4 x 0.18)

Lithography.

Silicon Wafer

Light Sensitive Coating.

Multiple Layers. >350 process steps.

Creating > 125 million transistors on each microprocessor;

With features 1/2000th the width of a human hair.
Evolution of technologies

First transistor (1949)
(Bardeen-Buddin Nobel 56)

SiGe Bipolar in 0.35µm monolithic process

First planar IC (1961)

5 µm MOSFET (1985)

15 nm MOSFET (2005)
Evolution of CMOS technologies

Moore's law: doubling every 2 years
Goal: Over 1 billion transistors by 2005

<table>
<thead>
<tr>
<th>Microprocessor</th>
<th>4004</th>
<th>8086</th>
<th>i386</th>
<th>Pentium</th>
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<td>16</td>
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<td>64</td>
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<td>10M</td>
<td>33M</td>
<td>66M</td>
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<tr>
<td>Mémoire adressable (bytes)</td>
<td>640</td>
<td>1M</td>
<td>16M</td>
<td>4G</td>
<td>64G</td>
</tr>
<tr>
<td>Technologie (µm)</td>
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<td>1</td>
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<td>0.18</td>
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<td>29000</td>
<td>275000</td>
<td>3.1M</td>
<td>42M</td>
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<tr>
<td>Tension alim (V)</td>
<td>12</td>
<td>5</td>
<td>5</td>
<td>5/3.3</td>
<td>1.3 interne</td>
</tr>
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</table>
« **CMOS scaling** »

- **Reduction of dimensions**
  - Gate length: \(L\)
  - Oxide thickness: \(t_{\text{ox}}\)

- **Reduction of power supplies**
  - Reduction of power dissipation

- **Improvement of speed in \(1/L^2\)**
  - Transconductance: \(g_m \propto W/L\)
  - Capacitance: \(C \propto WL\)
  - Speed: \(F_T = g_m / C \propto 1/L^2\)

- **Reduction of costs (?)**
  - Increase of integration density

- **Radiation hardness in bonus!**
  - Less trapping in gaye oxide

**Principle of N-channel MOSFET**
Evolution of CMOS technologies (2)

- Differences between analog/mixed signals and digital technologies
  - Very fast evolution of digital technologies (faster design migration)
  - More « perene » analog technologies (SiGe, BiCMOS...) (driven by mobile telecom and automotive)
  - A visible split occurring
- More difficult analog design in low voltage
  - « no more headroom for signals »

### Graphs

**Left Graph**
- **Gate length (µm)**
- Y-axis: gate length (µm)
- X-axis: year
- Data points for BiCMOS and CMOS technologies plotted over years 1980 to 2010

**Right Graph**
- **V_{CC} or V_{T} (V)**
- Y-axis: V_{CC} or V_{T} (V)
- X-axis: Technology Generation (µm)
- Plot showing (V_{CC} - V_{T}) and gate overdrive

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sept 2008 C. de La Taille Electronics in particle physics JoliotCurie08
Semiconductor Industry Roadmap
SiGe technology

- Faster bipolar transistors for RF telecom
  - Better mobility and FT
  - Better current gain (beta)
  - Better Early voltage
  - Interesting improvement at low T
  - Compact CMOS (0.25 or 0.35µm) for mixed-signal design
Cost of ASICs

- **MPW (multi-project wafers)**
  - CMOS 0.35µm (AMS) : 650 €/mm2
  - BiCMOS SiGe 0.35 µm (AMS) : 900 €/mm2
  - CMOS 0.13µ (STm) : 2500 €/mm2
  - CMOS 90 nm (STm) : 5000 €/mm2
  - Usually a few 10 to 100 pieces in a MPW run

- **Production runs**
  - Masks : 91 k€ (CMOS 0.35µm)
  - 8“ wafers : 4 k€, useful area : 25 000 mm2 = several thousands of chips

- **Packaging**
  - Ceramic : 20-30€/chip
  - Plastic : 2k€ + 1-2 €/chip

- **Example : chip 10mm² 16 channels**
  - 100 chips (MPW) : 120€/chip, 7€/channel
  - 10 000 chips (4 wafers) : 12€/chip < 1€/channel
(R)evolution of digital electronics (1)

- From stacks of circuits to FPGAs: programmable gate arrays

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Fastbus controller (1990)

Pentium processor board

2 FPGAs
(R)evolution of digital electronics (2)

- **Schematic -> High level languages (Verilog, VHDL)**
  - Example 8 bit comparator
  - 74LS866

- **VHDL comparator**:

  ```vhdl
  entity comparator_8 is
  port (  raz : in std_logic;
          val1,val2 : in std_logic_vector(7 downto 0)
          result : out std_logic
          );
  end entity comparator_8;
  architecure archi_1 of comparator_8 is
  begin
    result <= '0' when raz = '0' else
              '1' when val1 > val2 else
              '0'
  end architecture archi_1;
  ```
(R)evolution of digital electronics (3)

- **Reduction of digital logic levels**
  - 1980: TTL: 0-5 V
  - 2000: LVDS: Low Voltage (± 400 mV) Differential Swing
  - Better signal integrity (EMC)
  - Reduction of power supplies 5V → 3.3V → 2.5V → 1.2V

- **Components: the revolution of FPGAs:**
  - = Field Programmable Arrays (Altera©, Xilinx©)
  - 4-40 millions gates (55M in a Pentium4)
  - RISC 32bits processors
  - 10 Mbits resident memory
  - 2000 pins 1300 I/O (inputs/outputs)
  - 300 MHz operation
FPGAs as blackhole of digital electronics?

- RISC processors
- IP standard interfaces (Ethernet, USB, PCI...)
- Clocks & PLLs
- Matching networks
- DSP blocks, arithmetics
- Memories & FIFOs
- Bus interfaces (GTL, LVDS...)

©JP Cachemiche
Electromagnetic compatibility (EMC-EMI)

- Coexistence analog-digital
  - Capacitive, inductive and common-impedance couplings
  - A full lecture!
  - A good summary: there is no such thing as «ground», pay attention to current return
Effect of radiations on components

- **TID**: total ionising dose effects
  - Charge trapping in gate oxide
  - Alleviated in thin oxides (Deep SubMicron DSM)
  - Radiation tolerant layout techniques designed by CERN RD49 in 0.25µm
- **NIEL**: non ionising energy loss
  - Cristal damage with neutrons
  - Beta drop in bipolar transistors
- **SEU**: Single Event Effect
  - Effect of large ionising impact: local charge deposition on critical nodes
  - SEU: single event Upset = bit flip
  - SEL: single Event Latchup: thyristor setting -> destructive!
## Radiation hardness: space vs LHC

<table>
<thead>
<tr>
<th></th>
<th>Space missions</th>
<th>LHC experiments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mission Time</td>
<td>10-15 years</td>
<td>10 years</td>
</tr>
<tr>
<td>Service</td>
<td>Not Possible</td>
<td>Impractical</td>
</tr>
<tr>
<td>Electronics Reliability</td>
<td>High</td>
<td>High</td>
</tr>
<tr>
<td>Total Dose Requirements</td>
<td>10^-100 krad</td>
<td>1 krad - 10 Mrad</td>
</tr>
<tr>
<td>Non Ionizing Energy Loss (N)</td>
<td>~0</td>
<td>$10^{13-15}$ N/cm²</td>
</tr>
<tr>
<td>Single Event Upsets</td>
<td>IC's SEU characterised</td>
<td>No Critical SEU Accepted</td>
</tr>
</tbody>
</table>

=> Similar requirements
Examples and trends

- More pixels $\Rightarrow$ more integration
- System on chip $\Rightarrow$ more integration!
- 3D integration : still more integration!
MAROC : 64 ch MAPMT chip for ATLAS lumi

- Complete front-end chip for 64 channels multi-anode photomultipliers
  - Auto-trigger on 1/3 p.e. at 10 MHz, 12 bit charge output
  - SiGe 0.35 µm, 12 mm², Pd = 350mW
Active board pictures

MAROC2 chip bounded at CERN

64 ch PMT

MAROC side

Lattice side
MAROC Efficiency curves

![Graph 1](MAROC2 - USB 4 S-curves - all channels G1 Vdac = 1.35 V)

![Graph 2](MAROC2 - USB 4 S-curves - ch 12 - variable gain All channels at G1 Vdac = 1.36 V)

![Graph 3](trigger g 50 rms = 3.9 fC)

![Graph 4](MAROC2 - COB 4 Slow shaper waveforms vs gain All other ch: G1 (g16) Qinj = 100fC)
**MAROC 2: Charge output Wilkinson ADC**

- Measurements performed with the internal Wilkinson ADC
- Linearity of ±2% approximately

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**INTERNAL ADC**

![Graph 1](chart1.png)

![Graph 2](chart2.png)

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**MAROC2 - USB 4**

- Wilkinson ADC - 80MHz
- All channels at G1
- Mean pedestal vs channel number

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**MAROC2 - USB 4**

- Wilkinson ADC - 80MHz
- All channels at G1
- Pedestal RMS vs channel number

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**MAROC2 - USB 4**

- Wilkinson ADC - 80MHz
- All channels at G1
- Injected charge: 0 - 1.7 pC

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**MAROC2 - USB 4**

- Channel 0 - Gain 1 all ch
- Wilkinson ADC - 80MHz
- Mean reconstructed signal vs injected charge

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**MAROC2 - USB 4**

- Channel 0 - Gain 1 all ch
- Wilkinson ADC - 80MHz
- injected charge vs Amplitude (ADC counts)
PMm² : large photodetection area

- “PMm² (2006 - 2009), funded by the ANR: LAL, IPNO, LAPP and Photonis
- Replace large PMTs (20”) by groups of smaller ones (12”)
  - central 16ch ASIC (MAROC like)
  - 12 bit charge + 12 bit time
  - water-tight, common High Voltage
  - Only one wire out (DATA + VCC)
  - Target low cost
  - Reuse many parts from MAROC & SPIROC
- Application: large water Čerenkov neutrino
  - 1ns time resolution
  - High granularity
  - scalability
SPIROC : SiPM readout ASIC

- Silicon Photomultiplier Integrated Read Out Chip
  - Evolution from FLCSiPM
  - 36 channels
  - Charge measurement (15 bits)
  - Time measurement (< 1 ns)
  - Many SKIROC, HARDROC, and MAROC features re-used
  - Submitted in June 07 in SiGe 0.35 µm AMS

- Collaboration with DESY for ILC hadronic calorimeters
  - 9000 channels used in test beam in 2004-2008
  - Production in 2009 for Eudet module

Collaboration with DESY for ILC hadronic calorimeters

- 9000 channels used in test beam in 2004-2008
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SPIROC: one channel

- 8-bit DAC (0-5V)
- 1.5pF
- 0.1pF-1.5pF
- 15pF
- IN
- Low gain Preamplifier
- High gain Preamplifier
- Slow Shaper
- Fast Shaper
- Analog memory
- Variable delay
- Trigger
- Flag TDC
- 10-bit DAC
- TDC ramp 300ns/5 µs
- 4-bit threshold adjustment
- 12-bit Wilkinson ADC
- Conversion 80 µs
- Analog output
- 50-100ns
- Hold
- Depth 16
- Depth measurement
- Charge measurement
- Time measurement
- Common to the 36 channels
- Gain selection
- 4-bit threshold adjustment
- 10-bit DAC
- TDC ramp 300ns/5 µs
- READ
- Conversion 80 µs
- Analog output
SPIROC performance

- Good analog performance
  - Single photo-electron/noise = 8
  - Auto-trigger with good uniformity
  - Complex chip: many more measurements needed
Idef-X 2.E for ECLAIRs.

- 32 channels. Muxed output
- 2.2 mW/ch.
- Slow control => many parameters tunable
- Self triggered /1 Thresh/channel.
- 1µs-10µs selectable shaping.
- deal with both signal polarities.
- Peak detector, ~200mV/fC.
- sparsification and « smart » readout.

- Detector Leakage comp.
- Test/Calib inputs
- Channel Mask.

[Diagram of Idef-X 2.E for ECLAIRs]

Slow control -> RO sequencer

- Detector Leakage comp.
- Test/Calib inputs
- Channel Mask.
Idef-X: performances

Low Thresh. $\ll 4\text{keV}$

Production for flight model out from fab in may 2008
IDeF-X family: radiation hardness.

- **IDeF-X V1.0**

  - **TID**: Irradiation with $^{60}$Co @ 500rad/h up to 1 Mrad

  - Up to 1 Mrad: no visible effect excepted on noise performances => Noise increase cleared by annealing.

For ECLAIRs and SIMBOL-X (TID < 10krad)

New digital library to improve hardness against SEL:

Test on Idef-X V2.E => no anti latchup circuit required for the ECLAIRs mission.
CALISTE 64 : 3D Xray microcamera for SIMBOL-X

- A hybrid component based on a 3D Plus space proof technology.

- Four micro PCB perpendicular to detection plan.
- Four ASICs to read out 2 rows of eight pixels each.
- Lateral routing to share signals between ASICs.

CdTe detector
(64 pixels, 1mm pitch, 1mm thick, guard ring)

Front-end electronics
(4 IDeF-X 1.1 ASIC of 16 analogue channels)

Rear interface
(7x7 pin grid array, 1.27 mm pitch)

X radiography
3D technology

- Increasing integration density, mixing technologies
- Wafer thinning to <50 µm
- Minimization of interconnects
- Large industrial demand
  - Processors, image sensors…
3D technologies

- **Wafer stacking**

  - **Die to Wafer bonding**
    - Permits use of different size wafers
    - Lends itself to using KGD (Known Good Die) for higher yields

  - **Wafer to Wafer bonding**
    - Must have same size wafers
    - Less material handling but lower overall yield
ICV : Inter-Chip vias

- Processes « via first » and « via last »
- Diameters : 1 µm to 50 µm
- Aspect ratio ~10

- Hole etching and chip thinning
- Via formation with W-plugs.
- Face to face or die up connections.
- 2.5 Ohm/per via (including SLID).
Conclusion

- A real move towards “smart sensors”

- micro-electronics getting closer to detector
  - Unavoidable with increase of channels number
  - Cost reduction

- Backend more and more integrated
  - Integration of ADC
  - Signal processing
  - Loading of parameters

- Coming up : 3D integration
- 4-side abuttable sensors